16 Bit Processor

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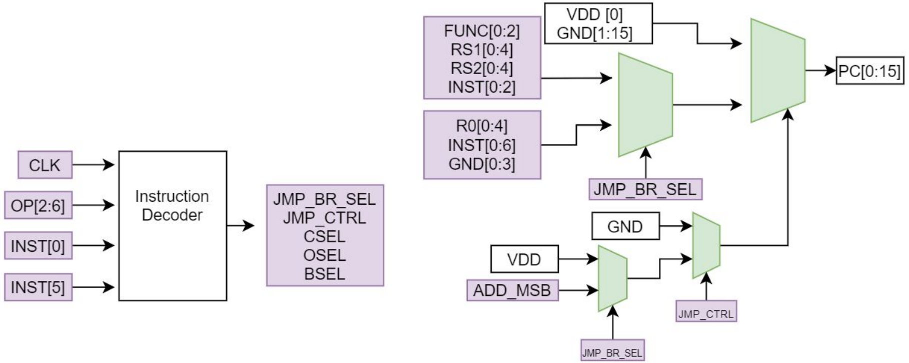
Introduction

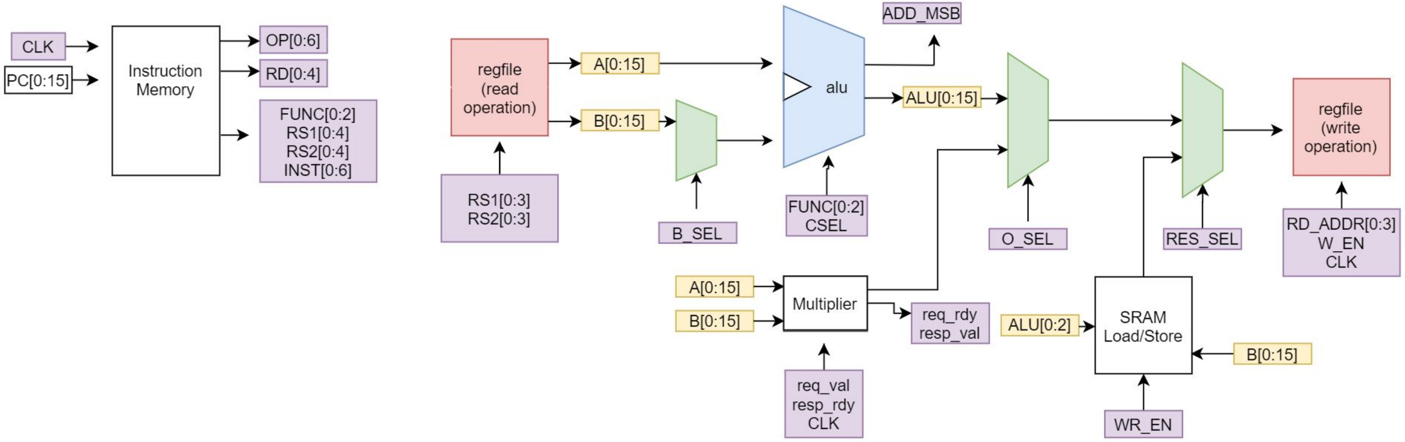
16 bit processor

- ALU
- Multiplier
- Read/Write SRAM Memory
- Register File
- Full System Architecture & Applications

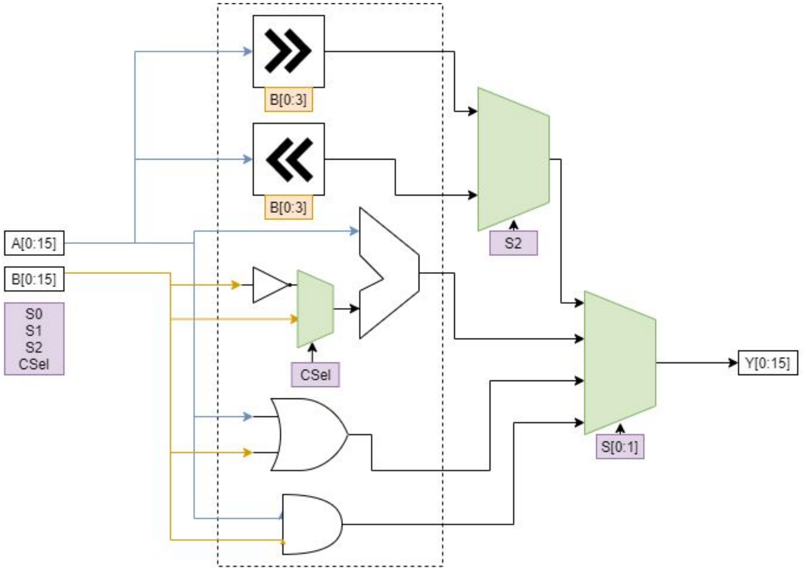
System Architecture

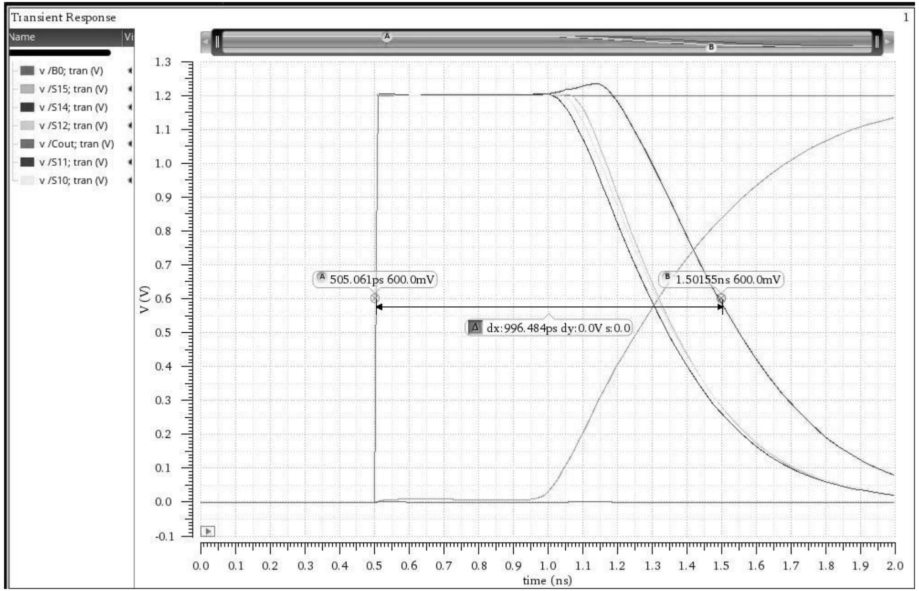


Instruction memory in verilog
Decoder in hardware (not laid out)



ALU Performance

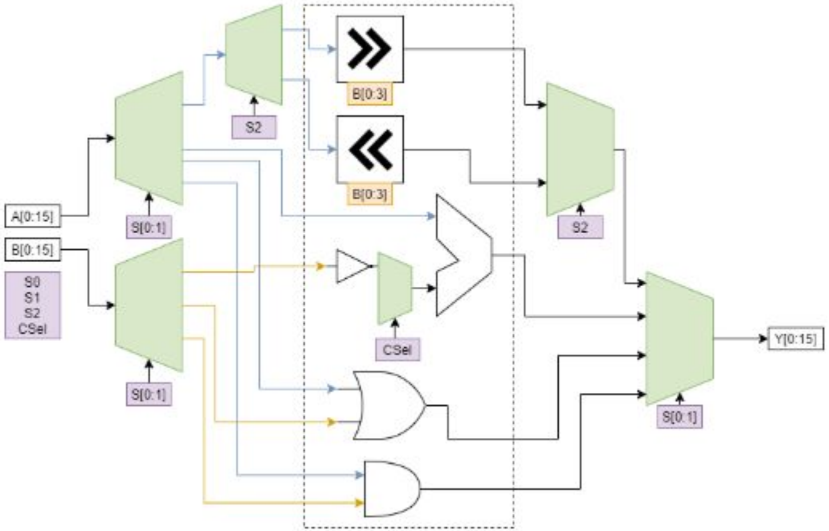




Metric	Result
Total Area (um^2)	4354
Max Delay (ps)	996
Max Current (mA)	10

- Add was the longest delay, worst case from lab
- Brent-Kung adder

ALU Comparison



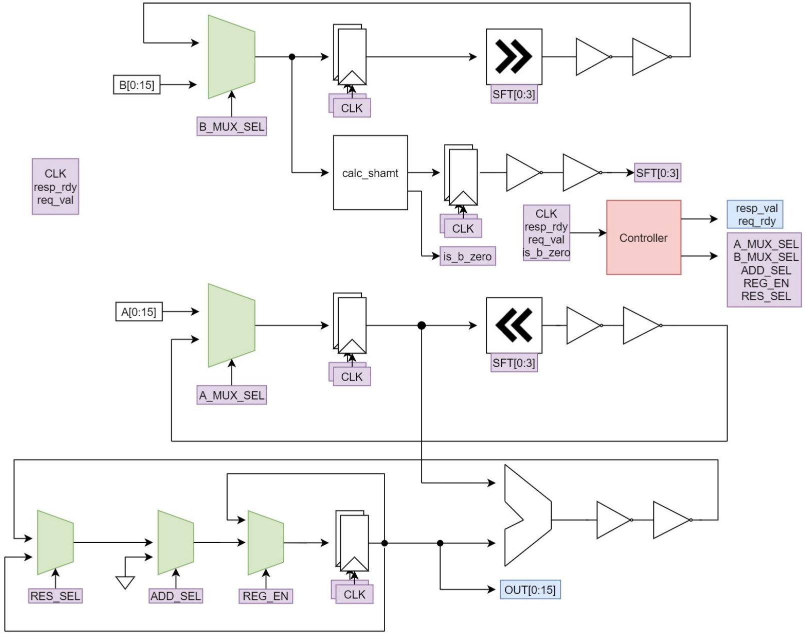
Metric	Base	Muxed Input
Total Area (um^2)	4354	5919
Max Delay (ps)	996	1030
Power Consumed (mW)	.053mW	.27mW

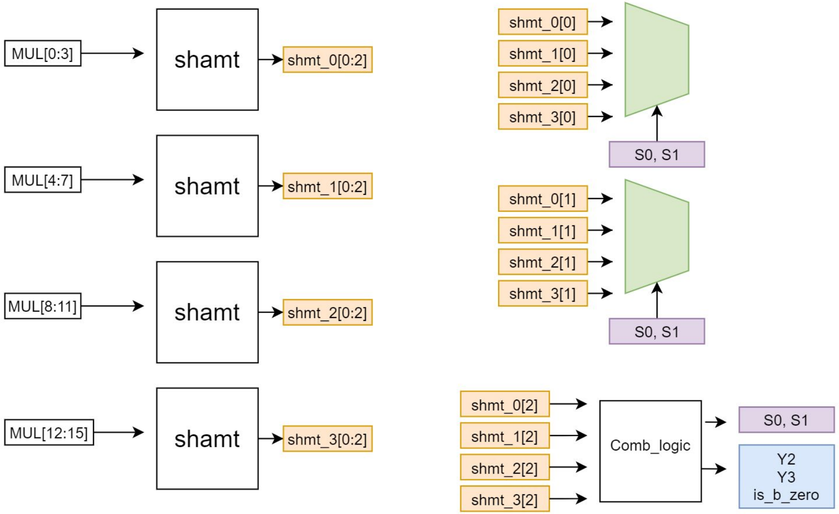
Goal: improve power by reducing dynamic power switching

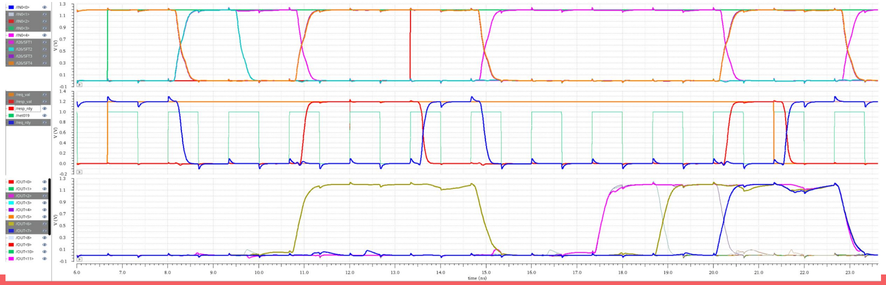
Current was higher overall due to DC, would have been better to power gate

Delay not too much higher due to lower fanout

Multiplier Performance

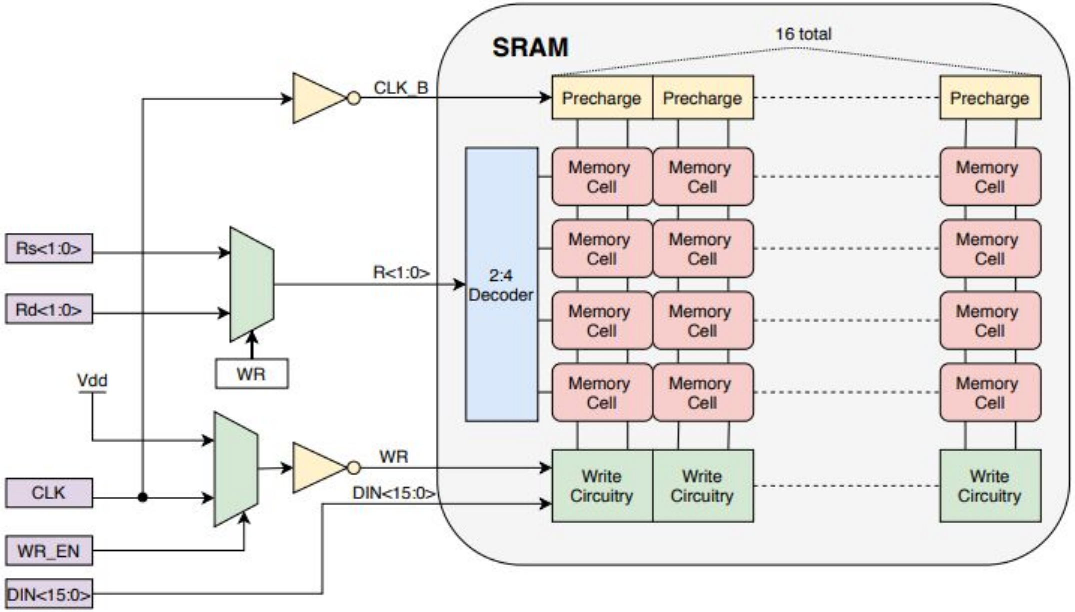






Metric	Result
Total Area (um^2)	10,984
Max Delay (ps)	1333
Peak Current (mA)	10.78

Read/Write Memory Performance



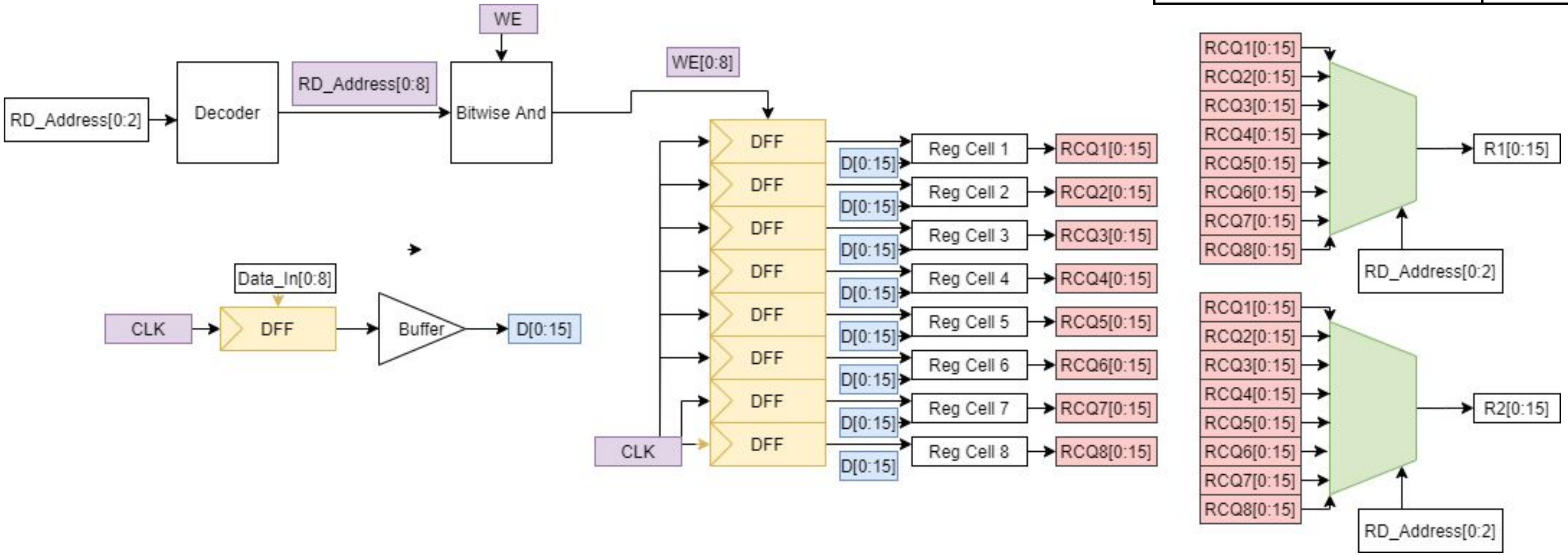
Metric	Result
Total Area (um^2)	700.2
Max Delay, Reading (ps)	25 **(loosely)
Peak Current (mA)	3.78

- Four 16-bit entries
- SRAM
- Ratio’d logic

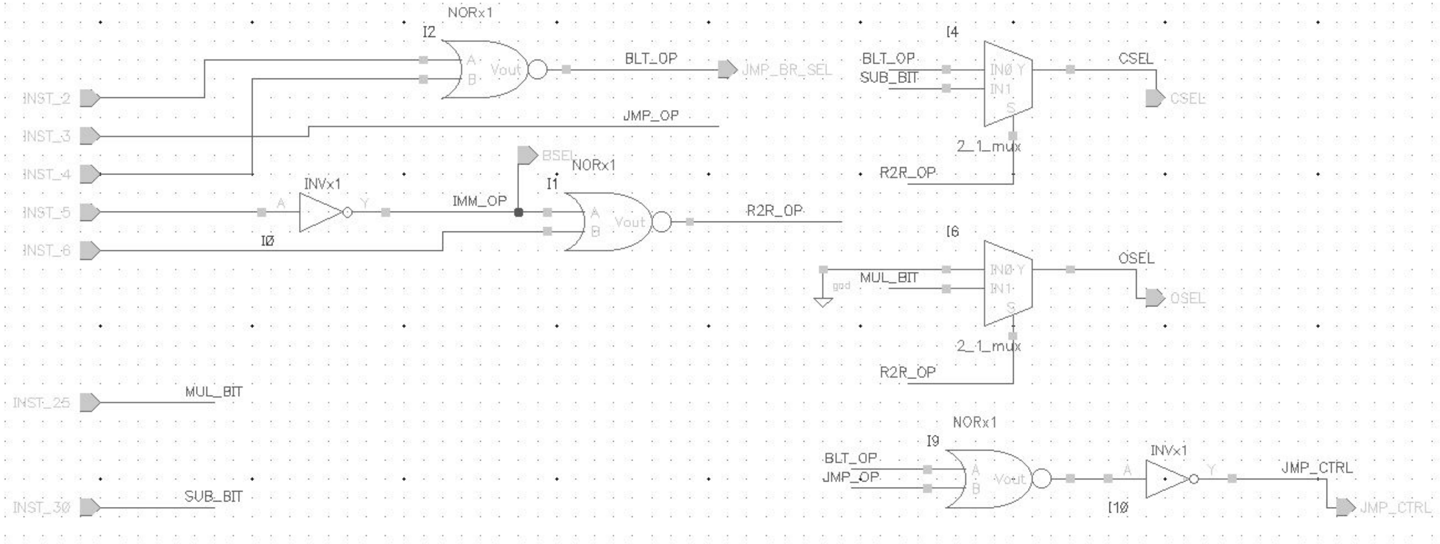
Reg File Performance

- Sub blocks laid out, not full layout
- WE and RD address AND to enable writing DFFs
- Can read two regs and write in same cycle
- 8 total registers

Metric	Result
Total Area (um^2)	7266
Max Delay (ps)	297.5
Peak Current (mA)	9.8



ISA/Test Bench



ISA from Comp Arch, 32 bit instructions mapped to 16 bit operations

Instructions stored as machine code inside a Verilog block (Instruction ROM)

PC Register and PC adder both internal to instruction memory to reduce repeated blocks

Decode verilog instructions to control signals using dedicated hardware

Full System Performance (**Not fully laid out)

Operations Tested:

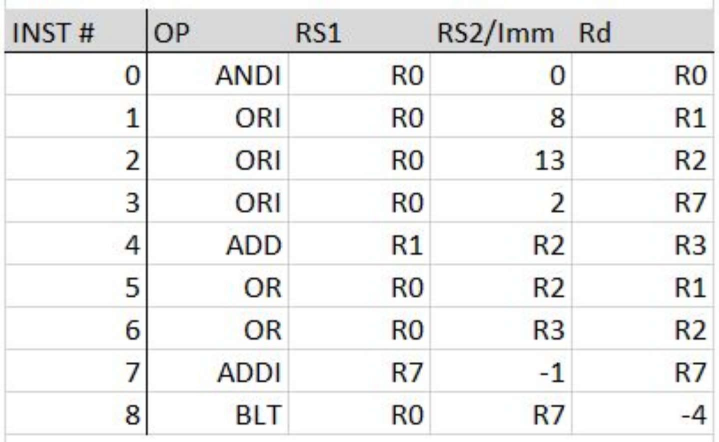
- Multiplying 3*4, R2R
- Add, subtract, OR, AND, shift
- Memory instructions
    - Store and Load
- Fibonacci

Metric	**Result**
Total Area	23,304 um^2
Max Theoretical Clock Frequency	600 MHz
Max Clock Frequency	200MHz
Max Current	10.78 mA

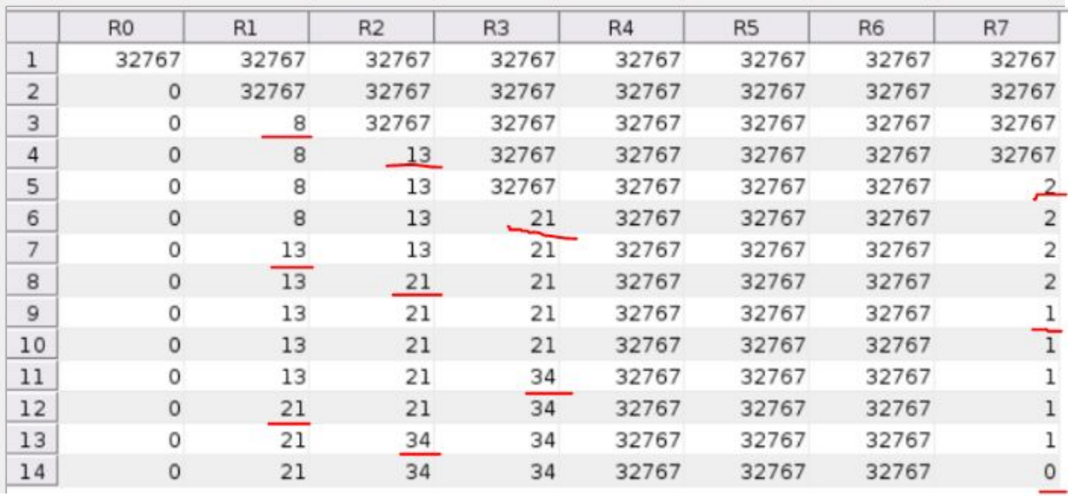
Real max frequency closer to 200MHz - adder was built with low drive strength (10fF), much higher when inputting to reg file

Full System Application

Finding the next two Fibonacci numbers in a sequence



INST #	OP	RS1	RS2/Imm	Rd
0	ANDI	R0	0	R0
1	ORI	R0	8	R1
2	ORI	R0	13	R2
3	ORI	R0	2	R7
4	ADD	R1	R2	R3
5	OR	R0	R2	R1
6	OR	R0	R3	R2
7	ADDI	R7	-1	R7
8	BLT	R0	R7	-4



	R0	R1	R2	R3	R4	R5	R6	R7
1	32767	32767	32767	32767	32767	32767	32767	32767
2	0	32767	32767	32767	32767	32767	32767	32767
3	0	8	32767	32767	32767	32767	32767	32767
4	0	8	13	32767	32767	32767	32767	32767
5	0	8	13	32767	32767	32767	32767	2
6	0	8	13	21	32767	32767	32767	2
7	0	13	13	21	32767	32767	32767	2
8	0	13	21	21	32767	32767	32767	2
9	0	13	21	21	32767	32767	32767	1
10	0	13	21	21	32767	32767	32767	1
11	0	13	21	34	32767	32767	32767	1
12	0	21	21	34	32767	32767	32767	1
13	0	21	34	34	32767	32767	32767	1
14	0	21	34	34	32767	32767	32767	0

Team Member Contributions

~Generally~

Katie - ALU

Alex - Top level design and testing, reg file

HJ - Read/write Memory

Anthony - Multiplier

Appendix A: layout pix